REMARKS

Claims 1-26 are pending. Claims 1-12 were rejected under 35 U.S.C. 102(e) as being anticipated by Theron (USP 6,631,520). Claims 13-26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Theron in view of Jacobson (USP 7,020,598).

It is respectfully submitted that Theron, taken alone or combined with Jacobson, does not teach or suggest all of the elements of the independent claims. The Examiner relies on Theron to teach or suggest "whereby said test logic is tested using said test routine under control of said microprocessor" in independent claim 1, "whereby said user logic is debugged using said debugging routine under control of said microprocessor" in claim 7, "executing said test routine under control of said microprocessor to test said programmable logic" in claim 13, and "executing said debugging routine under control of said microprocessor to debug said user logic" in claim 20.

Theron describes a system for configuring or testing a target FPGA. "An example system for configuring and/or testing target FPGA 10 from host system 20 using an interface device 30 in accordance with the present invention. Host system 20 is a conventional personal computer or workstation having a microprocessor such as, for instance, a Pentium processor available from Intel Corporation of Santa Clara, Calif. Although shown in FIG 3 as an FPGA, target device 10 is in some embodiments a chain of FPGAs or PLDs, and may in other embodiments be any other suitable programmable device(s). Further, target device 10 may have any suitable type of input port such as a JTAG-compatible port (set forth in the IEEE Standard 1149.1, "Test Access Port and Boundary Scan Architecture"), although other suitable port configurations may be used, e.g., a serial port, an express port, a peripheral port, synchronous port, asynchronous port, and so on." Theron does not teach or suggest using any test routine included in a programmable logic device memory to test user logic or test logic included in the programmable logic device. Theron only describes testing a target FPGA 10 using a host system 20 and an external interface 30.

It is respectfully submitted that Theron only describes a system similar to that described in the background section of the present invention. "Although the above techniques are useful, the increasing complexity of integrated circuits slows the speed at which testing and debugging of integrated circuits can occur. For example, during hardware emulation on chip, testing or

debugging may be slow. Testing or debugging is slow because of the speed of the external computer being used, the serial port on the device through which data and patterns must be passed, the necessary data gathering on the chip itself, and the presence of any probes used in the device. All these factors contribute to an emulation that becomes slower as chip complexity increases. One technique used for emulation available from Cadence and Synopsys involves a huge array of FPGAs in a hardware box. Numerous microprocessors load the FPGAs in order to simulate a hardware device for emulation. These emulation machines though, are extremely expensive." (page 2, lines 15-24)

By contrast, independent claim 1 recites "test logic", "whereby said test logic is tested using said test routine under control of said microprocessor." Theron does not teach or suggest any test logic whereby said test logic is tested using said test routing under control of said microprocessor. The target FPGA 10 in Theron is tested using an interface and external interface 30 and host system 20. Independent claim 7 recites "whereby said user logic is debugged using said debugging routine under control of said microprocessor." Claim 13 recites "executing said test routine under control of said microprocessor to test said programmable logic" in claim 13" and claim 20 recites "executing said debugging routine under control of said microprocessor to debug said user logic."

The target FPGA 10 in Theron is tested using an interface and external interface 30 and host system 20. At most, the Theron system possibly describes a testing an FPGA using an external processor. "Interface device 30 includes an on-board FPGA 32, a microcontroller 34, a static random access memory (SRAM) 36, and a serial programmable read-only memory (SPROM) 38. Interface device 30 also includes a Universal Serial Bus (USB) interface 40 and an RS-232 serial port interface 42, which are coupled to the USB and serial ports, respectively, of host system 20. On-board FPGA 32 is coupled to receive serial data from SPROM 38 via its serial port 32s, and is coupled to provide data to and receive data from SRAM 36 in a byte-wide parallel format via its parallel port 32p. Data is transferred between on-board FPGA 32 and microcontroller 34 via an address/data bus 33. On-board FPGA 32 and microcontroller 34 each provide control signals to one or more dedicated pins of the other via control lines, shown collectively in FIG 3 as a bidirectional bus 35, although actual embodiments may employ dedicated control lines. Microcontroller 34 is coupled to USB port 40 via a signal line 41 and to RS-232 serial interface 42 via a signal line 43." (page 4, lines 23-42)

CONCLUSION

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100